Course guide
2301220 - PMCASIC - Power Management Circuits in Asics

Last modified: 06/05/2024

Unit in charge: Barcelona School of Telecommunications Engineering
Teaching unit: 710 - EEL - Department of Electronic Engineering.

Degree: MASTER'S DEGREE IN SEMICONDUCTOR ENGINEERING AND MICROELECTRONIC DESIGN (Syllabus 2024). (Optional subject).

Academic year: 2024 **ECTS Credits:** 4.0 **Languages:** English

LECTURER

Coordinating lecturer: Consultar aquí / See here:

Others: Consultar aquí / See here:

PRIOR SKILLS

It is recommended that the student has been workin with the Cadence design environment previously. Basic knowledge of circuit analysis will be needed.

TEACHING METHODOLOGY

The course will combine lectures with problme solving sessions and laboratory work focused on specific problems to solve.

LEARNING OBJECTIVES OF THE SUBJECT

At the end of the course, the student should be able to choose the best power management circuit topologies for a given problem, knowing what the advantages and disadvantages of each circuit are. The student should also be able to identify what type of circuit has been used in an application by looking at its schematic. The student must have obtained the basic knowledge for the implementation using microelectronic design tools of these circuits.

STUDY LOAD

Type	Hours	Percentage
Hours large group	18,0	18.00
Self study	70,0	70.00
Hours small group	12,0	12.00

Total learning time: 100 h

CONTENTS

Block 1. Introduction to On-ichip Regulation and Power Management.

Description:
Basic review of architectures (main blocks) for DC/DC converters:
- References
- The switch
- Comparators
- Oscillators
- Protection Circuits

Low Voltage and high voltage approaches.

Full-or-part-time: 6h
Theory classes: 6h

Block 2. Inductor-less DC/DC converters

Description:
Linear Regulators (Low Drop-Out regulators)
- Bandgap voltage reference.
- PMOS switch architecture.
- Load and line regulation and stability.

Charge pumps

Full-or-part-time: 4h
Theory classes: 4h

Block 3. Inductor based DC/DC converters

Description:
Architectures
- Buck
- Boost
- Buck/Boost

Synchronous topology concept
Modes of operation: CCM/DCM
Combination of inductive DCDC and LDO

Full-or-part-time: 6h
Theory classes: 6h

Block 4. Power domains and floorplan

Description:
Power domains on ASIC.
Floorplan based on power distribution.

Full-or-part-time: 2h
Theory classes: 2h

GRADING SYSTEM

The final qualification will be obtaining by the weighted sum of different parts; the grade obtained by the evaluation of the reports generated in the different lab sessions (LAB), the grade obtained by questions and exercise proposed during class (EX) and the final exam.
The different weights will be: GRADE = 0.6*LAB + 0.2*EX + 0.2*TEST

BIBLIOGRAPHY

Basic:
- Hastings, A. The art of analog layout. 3rd ed. Pearson, 2023.
- Razavi, B. Design of analog CMOS integrated circuits. 2nd ed. Boston: McGraw-Hill, 2017. ISBN 9781259255090.
- Horowitz, P.; Hill, W. The art of electronics. 3rd ed. New York: Cambridge University Press, 2015. ISBN 9780521809269.