



# Course guide

## 2301205 - SOC - Soc Design and Verification

Last modified: 02/04/2024

**Unit in charge:** Barcelona School of Telecommunications Engineering  
**Teaching unit:** 1022 - UAB - (ANG) pendent.

**Degree:** MASTER'S DEGREE IN SEMICONDUCTOR ENGINEERING AND MICROELECTRONIC DESIGN (Syllabus 2024).  
(Optional subject).

**Academic year:** 2024    **ECTS Credits:** 6.0    **Languages:** English

### LECTURER

**Coordinating lecturer:** Consultar aquí / See here:  
<https://telecos.upc.edu/ca/curs-actual/coordinadors-i-professorat>

**Others:** Consultar aquí / See here:  
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### PRIOR SKILLS

Verilog HDL, C++, HW/SW Codesign, Computer Architecture, FPGA Design, ASIC back-end, Process Design Kits (PDK), Electronic Design Automation (EDA) tools

### TEACHING METHODOLOGY

Participatory Lectures. Resolution of exercises and problems. Laboratory practical work.

### LEARNING OBJECTIVES OF THE SUBJECT

This course is centered in the design and verification of complex System-on-a-Chip (SoC) components in a meet-in-the middle platform-based design approach, that builds complex chips out of SoC modules starting from predefined components and going down to both FPGA prototyping and ASIC layout. System-level HW/SW co-design tools are used for both specification, synthesis and verification, reinforcing specially that one as a key aspect of the design flow.

### STUDY LOAD

Type	Hours	Percentage
Self study	102,0	68.00
Hours large group	33,0	22.00
Hours small group	15,0	10.00

**Total learning time:** 150 h



## CONTENTS

### SoC Architectures

**Description:**

Elementary SoC architecture.  
Examples of processor cores (ARM, RISC-V). Pipeline.  
On-chip-buses (AMBA AXI OCB).  
Virtual Components (IPs).  
Memory Architecture.

**Full-or-part-time:** 31h 15m

Theory classes: 10h

Self study : 21h 15m

### Verification languages and methodologies

**Description:**

Verification concepts and methodologies. SystemVerilog for Verification. Simple and Complex testbenches. Co-simulation. Direct Programming Interface (DPI). Randomization and coverage (code and functional). Assertions.

**Full-or-part-time:** 31h 15m

Theory classes: 10h

Self study : 21h 15m

### High-level modelling languages and methodologies

**Description:**

SystemC TLM. Co-simulation SystemC-HDL. High-level synthesis tools.

**Full-or-part-time:** 28h 20m

Theory classes: 9h

Self study : 19h 20m

### SoC Back-end on FPGA & ASICs

**Description:**

FPGA prototyping. ASIC back-end. Packaging and test concerns.

**Full-or-part-time:** 12h 30m

Theory classes: 4h

Self study : 8h 30m

## Laboratory sessions

### Description:

1. SoC architectural customization (AXI, MMAP, IRQs, DMA,...) with virtual components (IPs)
2. SystemVerilog SoC testbench
3. Assertions, coverage, DPI
4. SystemC TLM HW/SW co-simulation of the SoC.
5. Synthesis to a SoC chip layout

### Specific objectives:

Students work with virtual components (IPs), connected to an integrated bus (OCB). The design of a specific SoC begins with the selection of its components and building its architecture, continues with functional verification at the level of individual components or small groups with SystemVerilog, followed by HW/SW co-simulation of the complete SoC with SystemC TLM, and ends with the synthesis of an ASIC that could be sent to manufacture.

### Related activities:

5 practical sessions of 3 hours each

**Full-or-part-time:** 46h 40m

Laboratory classes: 15h

Self study : 31h 40m

## GRADING SYSTEM

Individual assignments and activities (20%). Final exam (40%). Laboratory group work (40%, it is mandatory to pass it to pass the subject).

## BIBLIOGRAPHY

### Basic:

- Keating, M. The simple art of SoC design [on line]. New York, NY: Springer New York, 2011 [Consultation: 13/06/2024]. Available on: <https://link-springer-com.recursos.biblioteca.upc.edu/book/10.1007/978-1-4419-8586-6>. ISBN 9781441985866.
- Patterson, D.; Waterman, A. The RISC-V reader: an open architecture atlas [on line]. San Francisco: Strawberry Canyon, 2017 [Consultation: 11/06/2024]. Available on: <http://riscvbook.com/>. ISBN 9780999249116.
- Spear, C.; Tumbush, G. SystemVerilog for verification: a guide to learning the testbench language features [on line]. 3rd ed. New York, NY: Springer, 2012 [Consultation: 11/06/2024]. Available on: <https://link-springer-com.recursos.biblioteca.upc.edu/book/10.1007/978-1-4614-0715-7>. ISBN 9781461407157.
- Kogel, T.; Leupers, R.; Meyr, H. Integrated system-level modeling of network-on-chip enabled multi-processor platforms [on line]. Dordrecht, The Netherlands: Springer, 2006 [Consultation: 13/06/2024]. Available on: <https://link-springer-com.recursos.biblioteca.upc.edu/book/10.1007/1-4020-4826-2>. ISBN 9781402048258.

### Complementary:

- Chakravarthi, V.S. A practical approach to VLSI system on chip (SoC) design: a comprehensive guide [on line]. 1st ed. 2020. Cham: Springer Cham, 2020 [Consultation: 11/06/2024]. Available on: <https://link-springer-com.recursos.biblioteca.upc.edu/book/10.1007/978-3-030-23049-4>. ISBN 9783030230494.
- Flynn, M.J.; Luk, W. Computer system design: system-on-chip [on line]. Hoboken: Wiley, 2011 [Consultation: 11/06/2024]. Available on: <https://ebookcentral-proquest-com.recursos.biblioteca.upc.edu/lib/upcatalunya-ebooks/detail.action?pq-origsite=primo&docID=693260>. ISBN 9781118009901.
- Greaves, D.J. Modern system-on-chip design on arm [on line]. Arm Education Media, 2021 [Consultation: 11/06/2024]. Available on: <https://www.arm.com/resources/education/books>. ISBN 9781911531364.
- Beuchat, R.; Depraz, F.; Kashani, S.; Guerrieri, A. Fundamentals of system-on-chip: design on arm cortex-M microcontrollers [on line]. Arm Education Media, 2021 [Consultation: 11/06/2024]. Available on: <https://www.arm.com/resources/education/books>. ISBN 9781911531333.
- Mehta, A.B. ASIC/SoC functional design verification [on line]. Springer, 2017 [Consultation: 11/06/2024]. Available on: <https://link-springer-com.recursos.biblioteca.upc.edu/book/10.1007/978-3-319-59418-7>. ISBN 9783319594187.



- Wile, B.; Goss, J.C.; Roesner, W. Comprehensive functional verification: the complete industry cycle [on line]. 1st ed. Amsterdam ; Boston: Elsevier/Morgan Kaufmann, 2005 [Consultation: 13/06/2024]. Available on: <https://ebookcentral-proquest-com.recursos.biblioteca.upc.edu/lib/upcatalunya-ebooks/detail.action?pq-origsite=primo&docID=234976>. ISBN 9780080476643.
- Taraate, V. Digital logic design using Verilog: coding and RTL synthesis [on line]. 2nd ed. Singapore: Springer, 2023 [Consultation: 13/06/2024]. Available on: <https://link-springer-com.recursos.biblioteca.upc.edu/book/10.1007/978-981-16-3199-3>. ISBN 9789811946523.
- Herdt, V.; Drechsler, R.; Grosse, D. Enhanced virtual prototyping: featuring RISC-V case studies [on line]. Cham, Switzerland: Springer, 2021 [Consultation: 13/06/2024]. Available on: <https://link-springer-com.recursos.biblioteca.upc.edu/book/10.1007/978-3-030-54828-5>. ISBN 9783030548285.

## RESOURCES

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### Other resources:

IPs: Open source RISC-V processors, peripherals and tools  
EDA tools for design, verification and synthesis