Course guide
2301203 - PCR - Packaging, Characterization and Reliability

Last modified: 14/03/2024

Unit in charge: Barcelona School of Telecommunications Engineering
Teaching unit: 1022 - UAB - (ANG) pendent.

Degree: MASTER'S DEGREE IN SEMICONDUCTOR ENGINEERING AND MICROELECTRONIC DESIGN (Syllabus 2024). (Optional subject).

Academic year: 2024 **ECTS Credits:** 6.0 **Languages:** English

LECTURER

Coordinating lecturer: Consultar aquí / See here:

Others: Consultar aquí / See here:

PRIOR SKILLS

Course "Semiconductor Facilities and Device Manufacturing",

TEACHING METHODOLOGY

The methodology will combine master classes by the professors and hands-on exercises where the students will have to apply their knowledge to solve practical problems.

LEARNING OBJECTIVES OF THE SUBJECT

• Describe the basic packaging techniques of devices and circuits and select the best option based on the specifications and applications.
• Identify in-line and wafer-level characterization and analysis techniques for fabrication processes and devices specific to nanotechnology and describe their fundamentals, being aware of their limitations.

• Identify and describe the fundamentals of failure/aging mechanisms and variability in nanodevices. Design accelerated reliability tests for lifetime estimation in nanoelectronics.

• Describe failure analysis techniques for technology assessment and gain hands-on experience.

STUDY LOAD

Type	Hours	Percentage
Self study	102,0	68.00
Hours large group	30,0	20.00
Hours small group	18,0	12.00

Total learning time: 150 h

CONTENTS

Block 1. Packaging of devices and circuits

Description:
1.1 Introduction: Need for packaging. Single chip packages. Commonly used packages. Device Packaging types: THD (Through Hole Device), SMD (Surface Mounted Device), CSP (Chip Scale Packaging).
1.2 Materials and techniques. Wafer preparation and dicing. Die attaching. Wire bonding. Materials: metal, ceramics, polymers, glasses. Thermal behaviour and thermal mismatching.
1.3 Advanced packaging. Flip chip Bump Bonding. Current trends in packaging. Multichip modules (MCM). Hybrid circuits. System in package (SIP). Packaging roadmaps.
1.4 Issues. Parasitic resistance and capacity. Crosstalk. Power dissipation. Manufacturability. Testability. Reliability. Know Good Die problem. Lead-free alloys. Green electronics and RoHS compliance.

Related activities:
Master classes.

Full-or-part-time: 4h
Theory classes: 4h

Block 2. Electrical characterization of processes and MOS devices

Description:
2.1 Characterization of the fabrication process. In-line measurements (profilometry, interferometry, ellipsometry, 4-point probe, …). Test structures. Resistivity profiling by Differential Hall Effect and Spreading Resistance. Contact resistance measurements. Process qualification from C-V and current measurements (EOT, interfacial state density, Cox, flat band voltage…).

2.2 Electronic measurement systems for processes and devices characterization: wafer-probe stations, Source-Measurement Units, Semiconductor Parameter Analysers, C-V meters… Performance and limitations.

2.3 MOSFET performance evaluation: determination of performance parameters (threshold voltage, mobility, subthreshold swing….). Yield and process variability. Tests and test structures for compact model parameter extraction.

2.4 Reliability assessment

2.4.1 General concepts. Quality and reliability. Reliability modelling. Reliability of simple systems. Statistical distributions for reliability. Reliability of complex systems.

2.4.2 Reliability tests. Concept of reliability test. Accelerated tests. Introduction to Reliability Prediction Engineering.

2.4.3 Reliability in micro/nanoelectronics. Degradation/failure mechanisms in MOSFETs: Bias Temperature Instabilities, Hot Carrier Injection, Time-Dependent Dielectric Breakdown. Lifetime prediction. Other failure mechanisms: electromigration and ESD. Impact of CMOS scaling: time-dependent variability (TDV). Test structures, statistical characterization and modelling of the TDV. Reliability Simulation of integrated circuits: compact Models for TDV and Design for Reliability.

Related activities:
Master classes and hands-on work.

Full-or-part-time: 24h
Theory classes: 24h

Block 3. Failure analysis

Description:
Fault location on the surface of an IC. Structural analysis and possible effects on its operation. Reconstruction of functionality and proposal of actions that mitigate/prevent/solve possible failures.

Full-or-part-time: 2h
Theory classes: 2h

GRADING SYSTEM

Final exam (40%) + Course work (60%)

BIBLIOGRAPHY

Basic:

- Ulrich, R.K.; Brown, W.D. Advanced electronic packaging. 2nd ed. Wiley-Interscience/IEEE, 2006. ISBN 9780471466093.
- Tummala, R.R.; Rymaszewski, E.J.; Klopfenstein, A.G. Microelectronics packaging handbook. 2nd ed. Kluwer Academic Publishers, 1997. ISBN 0412084317.
- Razeghi, M. Fundamentals of solid state engineering [on line]. 4th ed. Cham: Springer International Publishing, 2019 [Consultation: 07/06/2024]. Available on: https://link-springer-com.recursos.biblioteca.upc.edu/book/10.1007/978-3-319-75708-7. ISBN 9783319757087.
- Sun, Y.; Li, L.; Tiniakov, D. Reliability engineering. Springer, 2023. ISBN 9789819959778.
- MacPherson, J.W. Reliability physics and engineering: time-to-failure modeling. 3rd ed. Springer, 2019. ISBN 9783319936826.
- Selecting the right SMU. White paper, Keysight Technologies, 2023.
- Strong, A.W. [i 6 més]. Reliability wearout mechanisms in advanced CMOS technologies. Wiley-IEEE Press, 2009. ISBN 9780471731726.
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- Bazu, M.I.; Bajenescu, T.I. Failure analysis: a practical guide for manufacturers of electronic components and systems [on line]. Chichester, West Sussex, U.K: Wiley, 2011 [Consultation: 21/06/2024]. Available on: https://onlinelibrary-wiley-com.recursos.biblioteca.upc.edu/doi/book/10.1002/9781119990093. ISBN 9781119990093.