# Course guide
# 2301200 - MD - Microelectronic Design

**Last modified:** 22/03/2024

**Unit in charge:** Barcelona School of Telecommunications Engineering
**Teaching unit:** 701 - DAC - Department of Computer Architecture.

**Degree:** MASTER'S DEGREE IN SEMICONDUCTOR ENGINEERING AND MICROELECTRONIC DESIGN (Syllabus 2024). (Compulsory subject).

**Academic year:** 2024 **ECTS Credits:** 6.0 **Languages:** English

## LECTURER

**Coordinating lecturer:** Consultar aquí / See here: https://telecos.upc.edu/ca/curs-actual/coordinadors-i-professorat

**Others:** Consultar aquí / See here: https://telecos.upc.edu/ca/curs-actual/coordinadors-i-professorat

## PRIOR SKILLS

General concepts on electronics, solid state technology and digital systems
- MOSFET behavior
- Digital electronics
- DC and transient analysis of circuits

## TEACHING METHODOLOGY

- Lectures
- Practical lab exercises
- Final test
- Autonomous work of the student

## LEARNING OBJECTIVES OF THE SUBJECT

Analyze and design the basic elements that constitute a digital microelectronic circuit from schematics to layout.
Use commercial Electronic Design Automation (EDA) tools for VLSI analysis and design.
Use advanced design techniques to optimize power consumption on IC's.
Introduction to VLSI technology independent high-level design methodologies and hardware description languages.

## STUDY LOAD

| Type | Hours | Percentage |
|---|---|---|
| Self study | 102,0 | 68.00 |
| Hours small group | 12,0 | 8.00 |
| Hours large group | 36,0 | 24.00 |

**Total learning time:** 150 h

## CONTENTS

### Introduction

**Description:**
Moore's Law. Evolution of VLSI technology.
Types of transistors for VLSI technology: planar MOSFET, FDSOI and FinFET. Principal characteristics and models for digital design.
Methodology and design flux. Hardware description languages.

**Full-or-part-time:** 12h 30m
Theory classes: 4h
Self study : 8h 30m

### Design of combinational blocks

**Description:**
The static CMOS logic gate.
Layout of static CMOS logic gates.
Logic gate characterization.
RC delay model.
Logical effort. Delay of digital blocks and paths.
Power consumption. Dynamic and static power.

**Related activities:**
Design and characterization of standard combinational cells

**Full-or-part-time:** 37h 30m
Theory classes: 8h
Laboratory classes: 4h
Self study : 25h 30m

### Design of sequential blocks

**Description:**
Latches and flip-flops. Characterization. Setup and hold time.
Design, layout and analysis of flip-flops. D-type and T-type flip-flops. Reset and enable signals.
Analysis and timing of digital circuits. Clock skew.
Synchronizers and timing analysis. Slack.
Memories. Structure and layout of memories ROM, SRAM, DRAM and Flash.content english

**Related activities:**
Design and characterization of standard sequential cells

**Full-or-part-time:** 31h 15m
Theory classes: 6h
Laboratory classes: 4h
Self study : 21h 15m

### Datapath subsystems

**Description:**
Adders and subtractors.
Comparators.
Counters.
Coders.
Shifters.
Multipliers.

**Related activities:**
Design and simulation of a datapath subsystem

**Full-or-part-time:** 25h
Theory classes: 6h
Laboratory classes: 2h
Self study : 17h

### Interconnect

**Description:**
Interconnect modeling.
Interconnect impact on circuit performance.
Interconnect engineering.

**Full-or-part-time:** 12h 30m
Theory classes: 4h
Self study : 8h 30m

### Low-power consumption techniques

**Description:**
Low-power architectures. Clock gating and power gating.
Dynamic voltage and frequency scaling (DVFS)
Low-power technologies and techniques.

**Full-or-part-time:** 12h 30m
Theory classes: 4h
Self study : 8h 30m

**Special purpose subsystems**

**Description:**
Power distribution.
Generation and distribution of clock signals.
Input/output pads.
Test and characterization.
Packaging and cooling.
Latchup, electromigration, antenna effect and parasitics.

**Related activities:**
Input/output PADs

**Full-or-part-time:** 18h 45m
Theory classes: 4h
Laboratory classes: 2h
Self study : 12h 45m

## GRADING SYSTEM

Lab exercices: 25%
Final test: 75%

## BIBLIOGRAPHY

**Basic:**
- Weste, N.H.E.; Harris, D.M. CMOS VLSI design: a circuits and systems perspective. 4th ed. Boston: Addison Wesley, 2011. ISBN 9780321547743.
- Rabaey, J.M.; Chandrakasan, A.P.; Nikolic, B. Digital integrated circuits: a design perspective. 2nd ed. Upper Saddle River: Pearson Education, 2003. ISBN 9788131709146.
- Taraate, V. Digital logic design using Verilog: coding and RTL synthesis [on line]. 2nd ed. Singapore: Springer, 2022 [Consultation: 17/05/2024]. Available on: https://link-springer-com.recursos.biblioteca.upc.edu/book/10.1007/978-981-16-3199-3. ISBN 9789811631986.

**Complementary:**
- Baker, R.J. CMOS circuit design, layout, and simulation. Fourth edition. Hoboken, New Jersey: IEEE Press, 2019. ISBN 9781119481515.
- Tsividis, Y.; McAndrew, C. Operation and modeling of the MOS transistor. 3rd ed. New York : Oxford: Oxford University Press, 2011. ISBN 9780195170153.