Course guide
820241 - DMD - Digital Microelectronic Design

Last modified: 25/06/2024

Unit in charge: Barcelona East School of Engineering
Teaching unit: 710 - EEL - Department of Electronic Engineering.

Degree: BACHELOR'S DEGREE IN BIOMEDICAL ENGINEERING (Syllabus 2009). (Optional subject).
BACHELOR'S DEGREE IN CHEMICAL ENGINEERING (Syllabus 2009). (Optional subject).
BACHELOR'S DEGREE IN ELECTRICAL ENGINEERING (Syllabus 2009). (Optional subject).
BACHELOR'S DEGREE IN ENERGY ENGINEERING (Syllabus 2009). (Optional subject).
BACHELOR'S DEGREE IN INDUSTRIAL ELECTRONICS AND AUTOMATIC CONTROL ENGINEERING (Syllabus 2009). (Optional subject).
BACHELOR'S DEGREE IN MECHANICAL ENGINEERING (Syllabus 2009). (Optional subject).
BACHELOR'S DEGREE IN MATERIALS ENGINEERING (Syllabus 2010). (Optional subject).

Academic year: 2024 **ECTS Credits:** 6.0 **Languages:** English

LECTURER

Coordinating lecturer: Cosp Vilella, Jordi

Others: Segon quadrimestre:
JORDI COSP VILELLA - M11

PRIOR SKILLS

To have completed the course on Digital Electronics and Electronic Technology

DEGREE COMPETENCES TO WHICH THE SUBJECT CONTRIBUTES

Specific:
1. Design analogue, digital and power systems.

Transversal:
2. EFFICIENT ORAL AND WRITTEN COMMUNICATION - Level 3. Communicating clearly and efficiently in oral and written presentations. Adapting to audiences and communication aims by using suitable strategies and means.
3. EFFECTIVE USE OF INFORMATI0N RESOURCES - Level 3. Planning and using the information necessary for an academic assignment (a final thesis, for example) based on a critical appraisal of the information resources used.

TEACHING METHODOLOGY

The teacher will show digital integrated circuit (chip) analysis and design procedures and how to configure commercial programmable logic devices (FPGAs and CPLDs) and some exercices to be solved by students will be proposed during the course.
In parallel, at the lab, the student will learn how to use electronic design computer tools to perform its own designs and to settle the learned concepts during lecture sessions.
A small design project on a digital electronic circuit will be also developed and experimentally verified using high level design tools (VHDL).

LEARNING OBJECTIVES OF THE SUBJECT

To learn how to analyze and design electronic integrated digital circuits on aplications specific circuits (ASIC) or standard programmable logic devices (PLD) using high level hardware description languages.
To learn how to analyze and design the basic elements that constitute a digital electronic circuit.
To learn how to use the tools for Electronic Design Automation (EDA) that are available on the market.

STUDY LOAD

Type	Hours	Percentage
Self study	90,0	60.00
Hours large group	45,0	30.00
Hours small group	15,0	10.00

Total learning time: 150 h

CONTENTS

Introduction to Microelectronics

Description:
Introduction and basic concepts of microelectronic technology and design

Specific objectives:
To be introduced to microelectronic basics.

Related activities:
None

Related competencies :
CEEIA-24. Design analogue, digital and power systems.
04 COE N3. EFFICIENT ORAL AND WRITTEN COMMUNICATION - Level 3. Communicating clearly and efficiently in oral and written presentations. Adapting to audiences and communication aims by using suitable strategies and means.
06 URI N3. EFFECTIVE USE OF INFORMATI0N RESOURCES - Level 3. Planning and using the information necessary for an academic assignment (a final thesis, for example) based on a critical appraisal of the information resources used.

Full-or-part-time: 5h
Theory classes: 2h
Self study : 3h

High Level Hardware Description of Integrated Circuits (VHDL)

Description:
The VHDL language and its application to integrated digital circuit design
Concurrent statements
Sequential statements
Testbench generation
Restriction files generation
Digital design advanced concepts

Specific objectives:
To learn how to design digital systems using high level hardware descriptions.

Related activities:
Development of a digital design using the high level hardware description language VHDL and practical verification of its functionality on a programmable device (FPGA)

Full-or-part-time: 54h 30m
Theory classes: 19h
Laboratory classes: 7h
Self study : 28h 30m

Review of MOS Transistor Fundamentals

Description:
MOS transitor models and basic concepts
MOS transistor characteristic curves
Modes of operation
NMOS transistor vs PMOS transistor
The current source

Specific objectives:
To know the basics of MOS transitors and to be able to use correctly these models in circuit design and analysis.

Related activities:
To obtain the current-voltage curve of type N and P MOS transistors by simulations and extract their most important parameters.

Related competencies :
CEEIA-24. Design analogue, digital and power systems.
04 COE N3. EFFICIENT ORAL AND WRITTEN COMMUNICATION - Level 3. Communicating clearly and efficiently in oral and written presentations. Adapting to audiences and communication aims by using suitable strategies and means.
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Full-or-part-time: 18h
Theory classes: 4h
Laboratory classes: 2h
Self study : 12h

The microelectronic Process

Description:
Introduction
Description of the VLSI microelectronic process
The layout

Specific objectives:
To know what the manufacturing process of CMOS integrated circuits is and understand its implications on the behaviour and performance of this kind of circuits.

Related activities:
To draw an elementary microelectronic circuit layout.

Related competencies :
CEEIA-24. Design analogue, digital and power systems.
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Full-or-part-time: 10h
Theory classes: 4h
Self study : 6h

The MOS Inverter

Description:
CMOS inverter structure
DC inverter behaviour
Dynamic inverter behaviour

Specific objectives:
To understand the behaviour of a CMOS inverter, to be able to analyze its static and dynamic behaviour and to be able to design it according to a certain specs.

Related activities:
Design and verify the behaviour through simulations of a CMOS inverter.

Related competencies :
CEEIA-24. Design analogue, digital and power systems.
04 COE N3. EFFICIENT ORAL AND WRITTEN COMMUNICATION - Level 3. Communicating clearly and efficiently in oral and written presentations. Adapting to audiences and communication aims by using suitable strategies and means.
06 URI N3. EFFECTIVE USE OF INFORMATI0N RESOURCES - Level 3. Planning and using the information necessary for an academic assignment (a final thesis, for example) based on a critical appraisal of the information resources used.

Full-or-part-time: 21h 30m
Theory classes: 6h
Laboratory classes: 2h
Self study : 13h 30m

Static Logic Gates

Description:
Description of NAND and NOR static gates
DC behaviour of the NAND and NOR gates
Dynamic behaviour of NAND and NOR gates
AND-OR-INVERTER logic
CMOS transmission gate

Specific objectives:
To understand the behaviour of a CMOS logical gate, to be able to analyze its static and dynamic behaviour and to be able to design it according to a certain specs.

Related activities:
Design and verify the behaviour through simulations of a CMOS logic gate.

Related competencies :
CEEIA-24. Design analogue, digital and power systems.
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Full-or-part-time: 23h
Theory classes: 6h
Laboratory classes: 2h
Self study : 15h

Sequential Circuits

Description:
The RS latch
The level triggered latch
The edge triggered flip-flop

Specific objectives:
To understand the behaviour of a CMOS flip-flop, to be able to analyze its static and dynamic behaviour and to be able to design it according to a certain specs.

Related activities:
Design and verify the behaviour through simulations of a CMOS flip-flop.

Related competencies :
CEEIA-24. Design analogue, digital and power systems.
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Full-or-part-time: 18h
Theory classes: 4h
Laboratory classes: 2h
Self study : 12h

GRADING SYSTEM

Course grade: Design exercises 20%; Laboratory exercises: 40% Design project: 40%

EXAMINATION RULES.

It is required to have completed the laboratory and course exercises to pass the course.

BIBLIOGRAPHY

Basic:
- Money Harris, David; Harris, Sarah L. Digital design and computer architecture. 2nd ed. Amsterdam: Elsevier, cop. 2013. ISBN 9780123944245.
- Bhasker, Jayaram. A VHDL primer. 3a ed. Upper Saddle River, New Jersey: Prentice Hall, cop. 1999. ISBN 0130965758.

Complementary:
- Baker, R. Jacob. CMOS circuit design, layout, and simulation. 4th ed. Hoboken, New Jersey: IEEE Press : Wiley, 2019. ISBN 9781119481515.
- Johns, D.; Martin, K. Analog integrated circuit design. New York [etc.]: John Wiley, cop. 1997. ISBN 0471144487.
- Tsividis, Y. Operation and modeling fo the MOS transistor. 3rd ed. New York: Oxford : Oxford University Press, 2011. ISBN 9780195170153.
- Weste, Neil H. E.; Money Harris, David. Integrated circuit design. 4th ed. Boston [etc.]: Pearson education, cop. 2011. ISBN 0321696948.